



Mini-ADACSync

User's Guide

January 2010

Revision history

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1.0	January 2010	First version.

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Version 1.0

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Introduction

The Mini-ADACSync is a high-precision, GPS-based clock generator. It is designed for our line of SFF SDR development platforms. It needs no host device management—all you need to do is connect it to your development platform and you're done.

Organization

This guide is organized as follows:

[Product overview](#) presents the product at a glance.

[Hardware description](#) presents the major hardware elements of the product, including connectors and various other components.

[Specifications](#) regroups the major technical specifications of the Mini-ADACSync.

Conventions

In a procedure containing several steps, the operations that the user has to execute are numbered (1, 2, 3...). The diamond (◆) is used to indicate a procedure containing only one step, or secondary steps. Lowercase letters (a, b, c...) can also be used to indicate secondary steps in a complex procedure.

The abbreviation *NC* is used to indicate no connection.

Capitals are used to identify any term marked as is on an instrument, such as the names of connectors, buttons, indicator lights, etc. Capitals are also used to identify key names of the computer keyboard.

All terms used in software, such as the names of menus, commands, dialog boxes, text boxes, and options, are presented in **bold** font style.

The abbreviation *N/A* is used to indicate something that is not applicable or not available at the time of press.

Note

The screen captures in this document are taken from the software version available at the time of press. For this reason, they may differ slightly from what appears on your screen, depending on the software version that you are using. Furthermore, the screen captures may differ from what appears on your screen if you use different appearance settings.

Glossary of terms

Throughout this document, you will find references to the following terms. Refer to the following table as to their definitions.

Table 1 Glossary of terms

Term	Definition
Application programming interface (API)	An application programming interface is the interface that a computer system, library, or application provides to allow requests for services to be made of it by other computer programs or to allow data to be exchanged between them.
Base design	Empty design or template that is incapable of data processing and is not instantiated in the custom logic of the board’s FPGA.
Board software development kit	Abbreviated BSDK, this kit gives users the possibility to quickly become fully functional developing C/C++ or assembly code for the DSP, and HDL code for the FPGA through an understanding of all Lyrtech boards’ major interfaces.
Chassis	Refers to the rigid framework onto which the CPU board, Lyrtech development platforms, and other equipment are mounted. It also supports the shell-like case—the housing that protects all the vital internal equipment from dust, moisture, and tampering.
Computer communication development	Refers to developing custom communications applications to communicate with Lyrtech boards.
cPCI	Short for CompactPCI, refers to a 3U or 6U Eurocard-based industrial computer where the all boards are connected through a passive PCI backplane.
cPCI chassis system	Refers to the chassis-CPU board-case system.
cPCI CPU	Host CPU of the cPCI chassis system, responsible for processing and communications between the hardware in the cPCI chassis and the remote computer connected to the cPCI chassis system.
Default design	Design loaded by default on Lyrtech boards used for FPGA design.
Digital signal processing	Digital signal processing is the study of signals in a digital representation and the processing methods of these signals. The algorithms required for DSP are sometimes performed using specialized devices that use specialized microprocessors called digital signal processors (DSP).
Digital signal processor (DSP)	A digital signal processor is a specialized microprocessor designed specifically for digital signal processing, generally in real time.
Eurocard	Refers to a European standard format for printed-circuit boards that can be connected together in a standardized subrack.
HDL	Stands for hardware description language.
Host	A host is defined as the device that configures and controls a Lyrtech board. The host may be a standard computer or the CPU board of the cPCI chassis system where the Lyrtech board is installed. You can develop applications on the host for Lyrtech boards through the use of an application programming interface (API) that comprises protocols and functions necessary to build software applications. These API are supplied with the Lyrtech board.
Model-based design	Refers to all the Lyrtech board-specific tools and software used for development with the boards in MATLAB and Simulink and the Lyrtech model-based design kit(s).
Reception	Any data received by the referent is a reception. Abbreviated RX.

Term	Definition
Reference design	Blueprint of an FPGA system implanted on Lyrtech boards. It is intended for others to copy and contains the essential elements of a working system (in other words, it is capable of data processing), but third parties may enhance or modify the design as necessary.
Software development	Refers to development performed with and for the board with a software development kit. Software development for a board comes in three flavors: host software development, DSP software development, and FPGA software development.
Transmission	Any data transmitted by the referent is a transmission. Abbreviated TX.
VHDL	Stands for VHSIC hardware description language.
VHSIC	Stands for very-high-speed integrated circuit.

Technical support

Lyrtech Inc. is firmly committed to providing the highest level of customer service and product support. If you experience any difficulties when using our products or if it fails to operate as described, we suggest that you first consult the user's guide, and then, if you are still in need of assistance, visit our Web site at www.lyrtech.com and fill the support request form.

Before reading this user's guide and sending your registration card, note the serial number of your Mini-ADACSync, its software version number (found on the software CD-ROM), and its date of purchase. This information is necessary when you call for service.

Serial number _____

Software version _____

Date of purchase _____

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Product overview

This chapter presents an overview of the Mini-ADACSync's outstanding features and potential applications.

Outstanding features

The Mini-ADACSync can boast of the following features:

Precision clock synthesizer/synchronizer

The Mini-ADACSync features an outstanding clock distribution circuit. The main component of this circuit is an Analog Devices AD9511 integrated circuit. It features a high-precision PLL and an external VCO to synthesize acquisition and transmission rates. The Mini-ADACSync is also equipped with a local high-precision, 10 MHz reference clock, and it supports external references.

NavSync CW25-TIM GPS receiver module

The Mini-ADACSync is equipped with a timing optimized GPS. The *PulsePerSecond* (PPS) signal supplied by the GPS module is used as the period reference in monitoring and disciplining the local, high-precision, 10 MHz reference clock. Space/time coordinates are extracted from the GPS' NMEA messages and the coordinates are available for applications such as data logging on the GPIO-32 interface.

Potential applications

Even if this product is specifically designed for SFF SDR development platforms (to synchronize the acquisition module (ADACMaster III) and the RF module(s) with a GPS-disciplined clock), many systems can take advantage of a low-cost, high-precision clock. For example:

- Sample rates generation for ADC/DAC boards
- System clocks synchronization
- Remote systems synchronization through a common GPS reference clock.

The following are examples of typical SFF SDR development platform configurations:

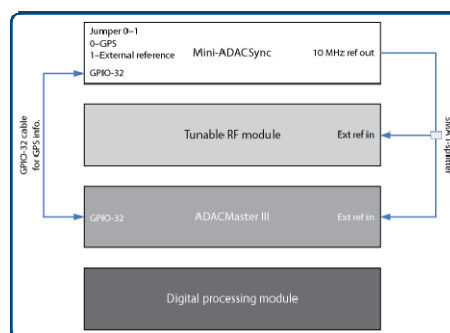


Figure 1 Tunable low/high-band SFF SDR development platform

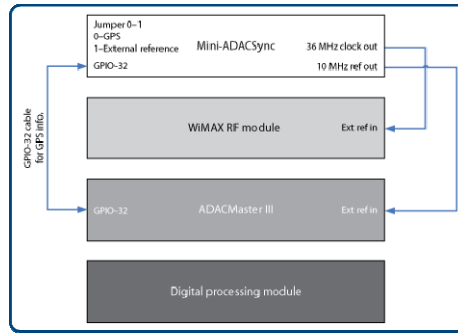


Figure 2 WiMAX SFF SDR development platform SISO configuration

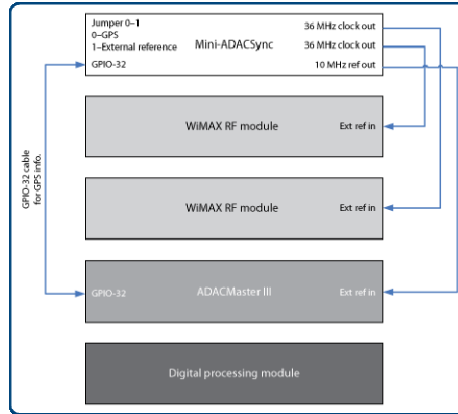


Figure 3 WiMAX SFF SDR development platform MIMO/dual-channel configuration

Development capabilities

You can use the module two different ways: with an external reference clock supplied by you or with the internal clock, generated from the GPS, high-precision time base (GPS-disciplined clock). Switching between modes is achieved by reconfiguring the jumpers on the module. See [Mini-ADACSync parts and functions](#) for details.

External reference clock

In this mode, the external clock is propagated to the AD9511 and used as the reference for clock generation. It is assumed that if you use this mode, it is because there is no available GPS RF signal; therefore, in this mode, the PPS out signal **does not** come from the GPS—it is rather a divided version of the external clock. It may be used for testing purposes.

Internal reference clock

In this mode, an internal 10 MHz clock is generated and used as a reference by the AD9511. The 10 MHz clock is GPS disciplined, meaning that the number of clock periods during a one-second period is counted; delimited by the PPS signal from the GPS. The generated clock frequency is then adjusted to match a count of 10,000,000. The GPS RF signal is necessary to operate in this mode; therefore, the PPS out signal comes from the GPS, through the FPGA.

Note

The adjustment value for the generated frequency is in the FPGA’s internal flash memory. It is updated approximately each 12.5 minutes, as long as there is a good GPS signal. This allows clock disciplining. Every time the Mini-ADACSync boots, the clock disciplining mechanism uses the value in the FPGA’s flash memory. This allows quick tests where there is no GPS RF signal readily available (based on the premise that this is the best possible value available, due to a lack of reference GPS RF signal).

Hardware description

This chapter presents an overview of the Mini-ADACSync at a hardware level.

Mini-ADACSync block diagram

The Mini-ADACSync can be represented by the following block diagram:

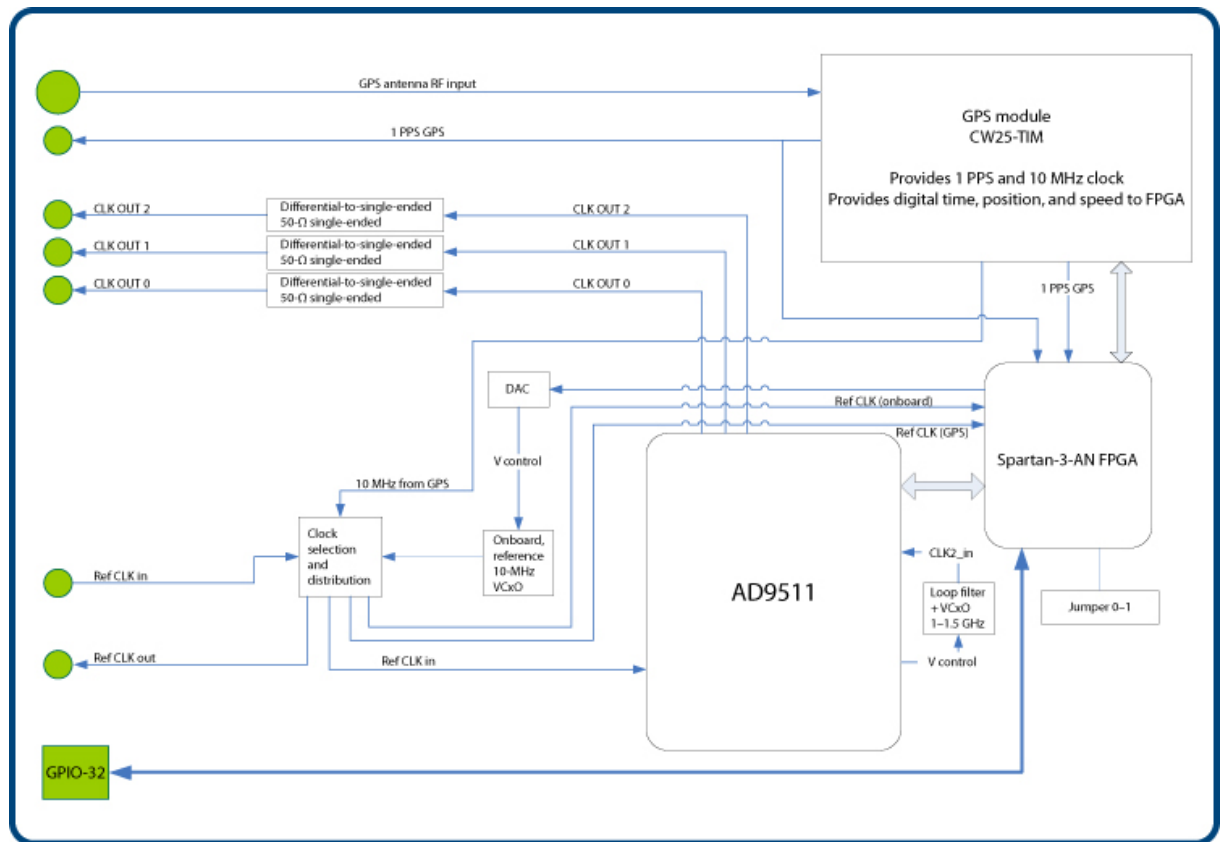


Figure 4 Mini-ADACSync block diagram

Mini-ADACSync parts and functions

Physically, the Mini-ADACSync is laid out as follows:

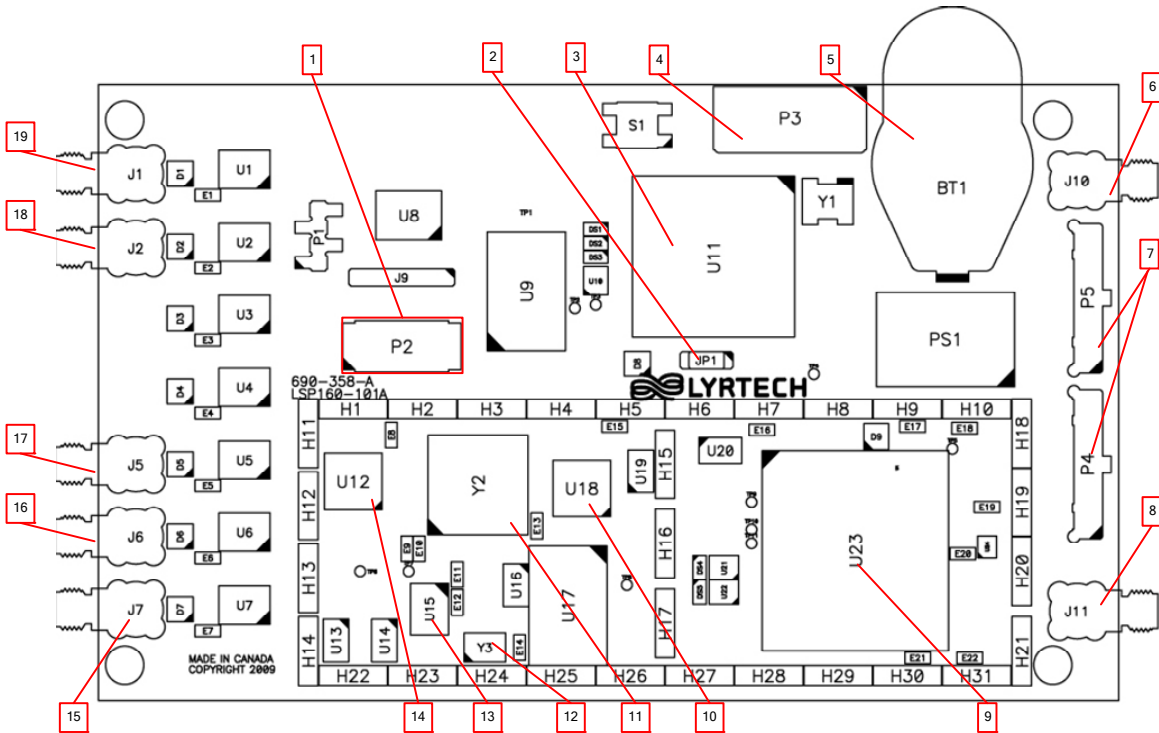


Figure 5 Mini-ADACSync top view

1. JTAG connectors

Flying lead and ribbon cable JTAG connectors.

2. Clock selection jumper

Use jumper JP1 to select a clock mode. Placing the jumper in position 1–2 selects the external reference source and placing it in position 2–3 selects the onboard reference clock.

Note

You must turn off and restart the SFF SDR development platform (or the Mini-ADACSync, if you are using it alone) before new jumper settings take effect.

3. FPGA

Xilinx Spartan-3 XC3S50AN-4TQG144C. Used to control various SPIs of the Mini-ADACSync with the GPS receiver and implement the reference clock’s correction logic.

4. GPIO-32 connector

Standard GPIO-32 connector used to transmit time and position information to other boards equipped with a GPIO connector. See [GPIO-32](#) for details about this interface.

5. Battery

Used to store time information when the CW25-TIM GPS receiver module (see [9](#)) is off (as the CW25-TIM receiver module is equipped with an onboard, real-time clock (RTC)). Having valid time information improves the time to first fix (TTFF).

6. Reference clock input connector

SMA jack. Used to connect an external reference, 10 MHz clock to the AD9511. This external reference clock is also supplied at the reference clock output connector (below).

7. Power supply connectors

Used to supply the module with power.

8. GPS antenna input connector

50 Ω , SMA jack. Used to connect a GPS antenna.

9. GPS receiver

NavSync CW25-TIM GPS receiver module. Used to supply time and position information, as well as a 1 PPS clock output used in adjusting the 10 MHz, onboard reference clock to a precision of 0.1 ppm.

10. Reference clock switch matrix

Used to select an onboard or external reference clock, and then distribute the selected clock to the FPGA (see [2](#)), PLL (see [14](#)), and reference clock output connectors.

11. VCO

1.0–1.5 GHz, high-quality voltage-controlled oscillator. Combined with the on-chip PLL of the AD9511 (see [14](#)), you can generate almost any frequency in the 31.25 MHz to 350 MHz range.

12. Onboard reference clock

When selected as a clock source, it is used as a precise reference for the AD9511 PLL (see [14](#)).

13. DAC

Used to adjust the onboard reference clock's control voltage (see [12](#)).

14. PLL

Analog Devices AD9511. The AD9511 have five outputs (outputs 0 to 4) only three of which are externally available. Each output has an independent clock divider allowing dividing the common VCO frequency by 1 to 32. Outputs 0 to 2 are fed to three differential-to-single-ended, 50 Ω drivers.

15. CLK0 output connector

SMA jacks. Used to connect to output 0 of the AD9511. Providing a 36 MHz clock.

16. CLK1 output connector

SMA jacks. Used to connect to output 1 of the AD9511. Providing a 36 MHz clock.

17. CLK2 output connector

SMA jacks. Used to connect to output 2 of the AD9511. Providing a 36 MHz clock.

18. Reference clock output connector

SMA jack. The AD9511 reference clock is also routed here.

19. 1-PPS output connector

SMA jack. Supplies the 1-PPS signal, from the GPS receiver in internal mode, and from the divided external clock in external mode.

Clock distribution circuit

The clock distribution circuit is based on the Analog Devices AD9511 device. The circuit is a high-performance, low phase-noise, low-skew clock synthesizer/synchronizer that synchronizes the onboard voltage-controlled oscillator (VCO) frequency with a reference clock. The Mini-ADACSync is equipped with a 0.1-ppm, 10 MHz reference clock that acts as a time base, and equipped with a high-quality VCO capable of frequencies between 1 GHz and 1.5 GHz.

GPIO-32

The digital input/output header of the Mini-ADACSync is a 32-bit parallel link (GPIO-32) capable of data transfers. As an output, the GPIO-32 header is used to supply you with a GPS space/time stamp. The GPS data and strobe are on ports DIO_0 to DIO_7 and DIO_28, respectively. The 32-bit, external GPIO-32 header is a Samtec, 14-pin FTSH-107-01-L-D-DH with the following pin assignments. (Pin 1 is adjacent to the cable’s red index mark.)

Table 2 GPIO-32 header pin assignments

Pin	GPIO-32 pin	Pin	GPIO-32 pin
1	DIO_0	2	DIO_1
3	GROUND	4	DIO_2
5	DIO_3	6	DIO_4
7	DIO_5	8	DIO_6
9	DIO_7	10	DIO_8
11	DIO_9	12	DIO_10
13	DIO_11	14	DIO_12
15	DIO_13	16	DIO_14
17	DIO_15	18	DIO_16
19	DIO_17	20	DIO_18
21	DIO_19	22	DIO_20
23	DIO_21	24	DIO_22
25	DIO_23	26	DIO_24
27	DIO_25	28	DIO_26
29	DIO_27	30	DIO_28
31	DIO_29	32	GROUND
33	DIO_30	34	DIO_31

The electrical level is 3.3 V CMOS.

Caution

Exercise caution when you use the *DIO_x* signals, because they are directly connected to the FPGA’s inputs and outputs and **there is no buffer between the FPGA and the connectors**. Overvoltage or contention can seriously damage the FPGA.

Connecting a GPIO-32 flat ribbon cable to the Mini-ADACSync

You can connect a GPIO-32 flat ribbon cable to the GPIO-32 header of the Mini-ADACSync. Take care to correctly align pin 1 of the cable and the header. The connector recessed from the PCB’s edge and there is no groove in the connector on the PCB to ensure that the cable is correctly inserted. Lyrtech recommends that you use a Samtec FFSD-17-D-12-01-N flat ribbon cable.

Note

Take care that the input/output setting is correctly configured before connecting the cable to other devices.

Onboard LEDs

FPGA_DONE

When it is lit, the LED indicates that the FPGA bitstream was successfully loaded.

PLL_LOCK

When it is lit, the LED indicates that the local PLL successfully achieved lock.

REF_CLK_LOCK

When it is lit, the LED indicates that:

- The PPS signal from the GPS is valid
- The internal control loop generating the 10 MHz, GPS-disciplined clock is in fine compensation mode
- The internal control loop that generates the 10 MHz, GPS-disciplined clock is within the tolerance range

Note

The REF_CLK_LOCK LED is only relevant when a GPS RF signal is present, as it is derived from the GPS outputs.

GPS red and green LEDs

For complete descriptions of the meaning of these LEDs, refer to NavSync's Web site at navsync.com where you will be able to locate the appropriate documentation.

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Specifications

This chapter presents the main technical specifications of the Mini-ADACSync.

Note

The specifications in this chapter are subject to change without notice.

Table 3 General specifications

Parameter	Minimum	Typical	Maximum
General specifications			
Supply voltages	–	12 V	–
Supply currents	–	0.34 A	–
Power consumption	–	4.08 W	–
Length	–	148 mm 160 mm (including connectors)	–
Width	–	88 mm 95 mm (including connectors)	–
AC/DC specifications			
Output clocks			
Buffered and independent programmable output clocks	–	3	–
Output impedance	–	50 Ω	–
Output type	–	Single-ended LVCMOS	–
Connectors	–	SMA	–
Clock generation range	31.25 MHz	–	350.00 MHz
VCO range	1.0 GHz	–	1.5 GHz
VCO+PLL resolution	–	100 kHz	–
Input/Output reference clocks			
Onboard VCXO frequency	–	10 MHz	–
Onboard VCXO precision	–	0.1 ppm (GPS disciplined) 2.5 ppm (free-running)	–
Onboard VCXO phase noise	–	–83 dBc/Hz, 10 Hz –115 dBc/Hz, 100 Hz –135 dBc/Hz, 1 kHz –140 dBc/Hz, 10 kHz	–
Input/Output reference clock impedance	–	50 Ω	–
Input/Output reference clock type	–	Single-ended LVCMOS	–
Input reference clock amplitude	8 dBm	10 dBm	12 dBm
Connectors	–	SMA	–

Parameter	Minimum	Typical	Maximum
Input/Output reference clock range	1 MHz	10 MHz	250 MHz

GPS specifications

Table 4 GPS specifications

Parameter	Specification
Antenna placement	Near windows (installation dependent) Outdoors
Type of antenna	3.3 V active antenna
Antenna input connector	SMA
Antenna input impedance	50 Ω
PPS output connector	SMA
PPS output impedance	50 Ω
Available GPS readout information at GPIO-32 connector	UTC time UTC day Latitude Longitude Altitude Speed over ground Course over ground
GPIO-32 interface—electrical	3.3 V LVCMOS
GPIO-32 interface—connector	Pitch 0.05 in. 2×17 header

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