

# ADACSync

## Multichannel, GPS-disciplined, precision clock generator

The ADACSync is a 6U, cPCI (PXI compatible), GPS-disciplined, precision, low-jitter clock generator featuring:

- 12 buffered output channels
- Five programmable clocks
- The possibility of an external or onboard reference clock
- A high-precision GPS reference clock option

These features make the ADACSync perfect in synchronizing multichannel system clocks.

The first programmable clock of the ADACSync (CLK0) is buffered and distributed to eight synchronous output channels, which allows synchronizing several digitizer boards or daisy chaining ADACSyncs for even more channels (with an external input clock). The four other programmable clocks (CLK1–CLK4) are independent, single-channel buffered outputs. CLK4's delay can also be tuned to perform precise adjustments.

The ADACSync is also equipped of a GPS module, providing a 10 MHz reference clock. An optional control-loop logic core allows the onboard 10 MHz VCxO to continuously and precisely match the GPS reference.

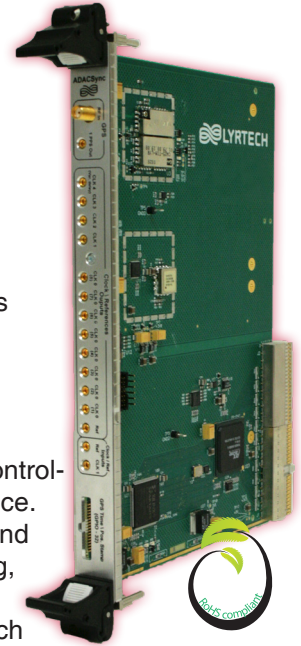
This ensures very-low-jitter clock distribution and tight alignment to the GPS reference allowing, for example, several remote acquisition systems to be synchronized (such as Lyrtech [VHS-ADCs](#) and [VHS-DACs](#)).

GPS position and time information can also be published through the GPIO-32 or cPCI interfaces for DAQ time/position-stamping applications, which perfectly matches Lyrtech's multichannel acquisition boards—the VHS-ADC, VHS-DAC, and [ADACMaster III](#).

### Applications

The following are only a few of the applications where the ADACSync truly shines:

- Generation of sample rates for ADC/DAC boards
- Synchronization of system clocks
- Synchronization of multichannel acquisition systems such as MIMO, OTH radar, and medical imaging systems
- Integration to clock distribution systems and data acquisition systems
- Synchronization of remote systems through a common GPS reference clock



### AT A GLANCE

- Five, independent programmable clock outputs
- Output range from 31.25 MHz to 350.00 MHz
- Less than 0.1 ppm, onboard VCxO, GPS-matched, precision reference
- Distribution buffer with eight frequency-aligned channels (programmable CLK0)
- Four, independently buffered outputs (programmable CLK1–CLK4)
- Reference clocks—External, onboard, or GPS
- Drives 50-Ω, single-ended loads
- Reference clock and 1 pps GPS outputs
- GPS time/position-stamp at GPIO-32 output
- Stand-alone configuration through onboard EEPROM
- Easy-to-use programming application
- Plug and Play with Lyrtech ADC/DAC boards

### Software tools

The ADACSync comes with an application used to configure and control the platform's parameters, as well as obtain GPS information from the cPCI and GPIO-32 interfaces.

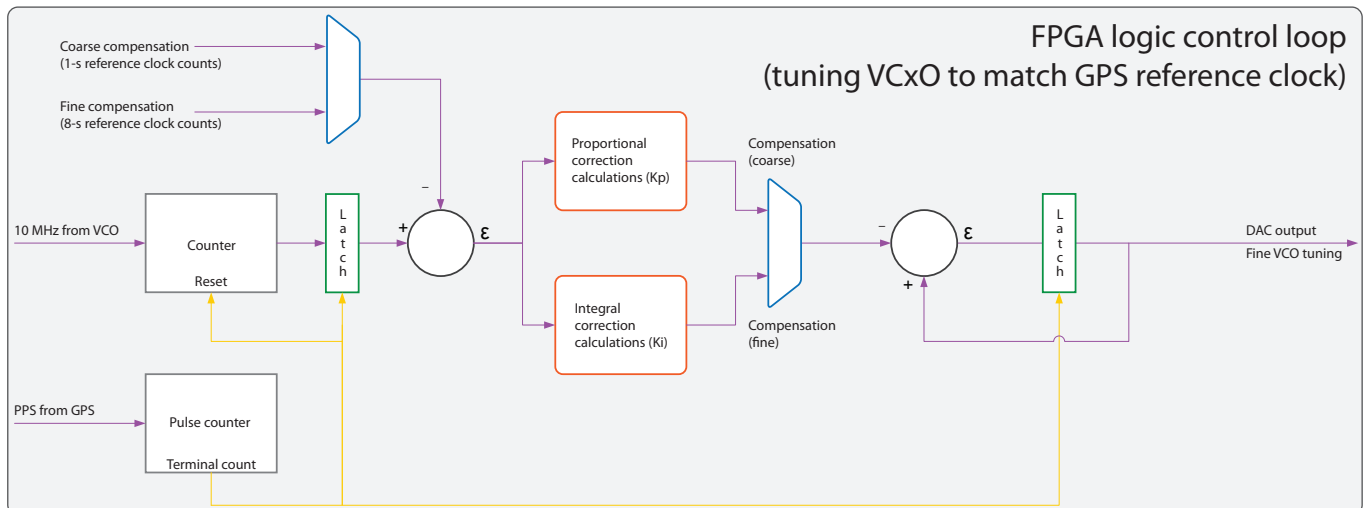
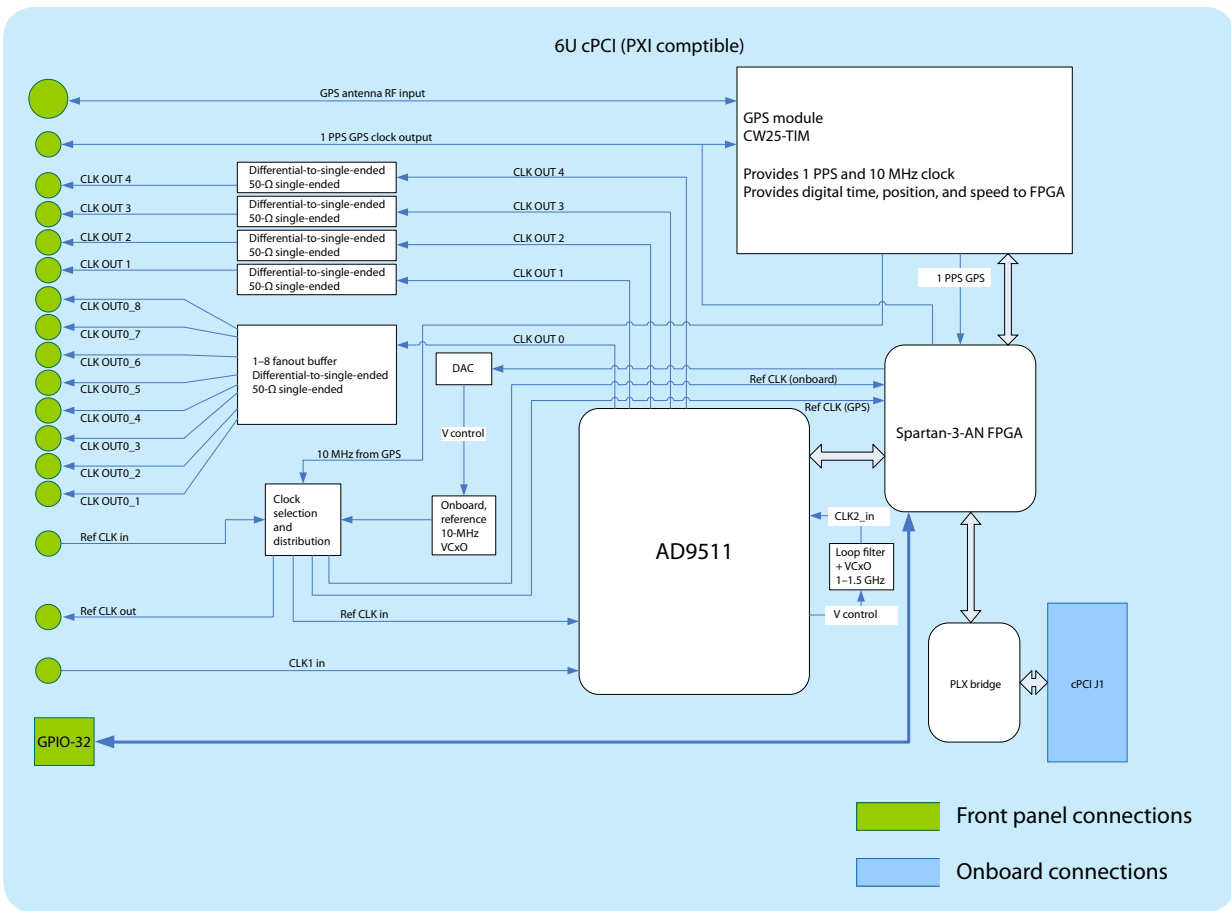
When all the platform's parameters are configured, a programming interface allows you to save the configuration setup in the EEPROM. The platform is thus able to boot itself, without any intervention from the PCI, making it completely stand-alone and independent from operating systems.

A thoroughly documented API also comes with the platform for you to develop your custom control interfaces. Developers working on Linux and VxWorks can also easily port the existing Microsoft Windows-based drivers with the simple, memory-map configurable registers.

# Specifications

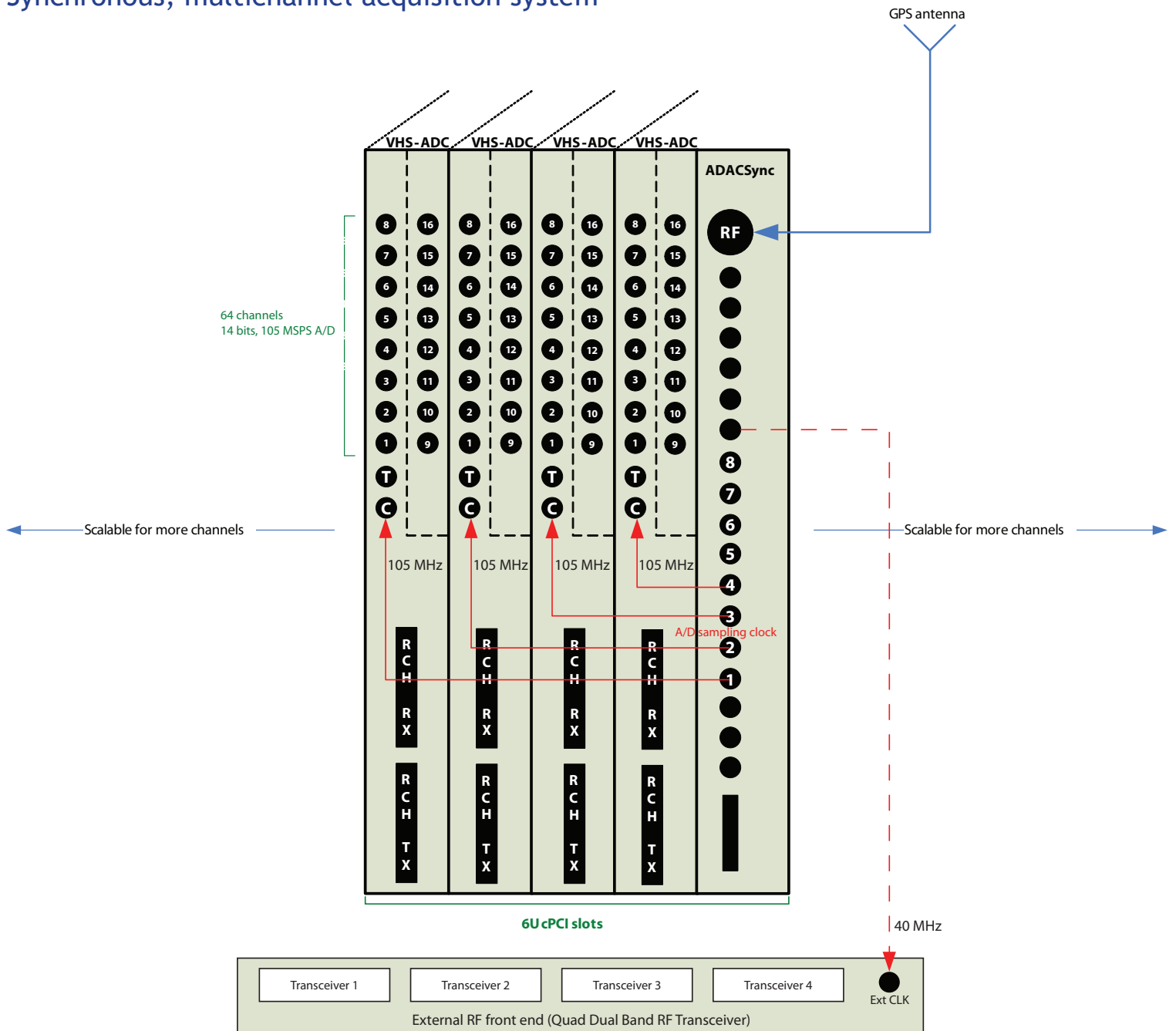
<b>Output clocks</b>	Buffered output clocks	12
	Buffered phased-aligned clocks	8
	Independent programmable clocks	5
	Output impedance	50 $\Omega$
	Output type	Single-ended LVCMOS
	Connectors	MMCX
	Clock generation range	From 31.25 MHz to 350.00 MHz
	Clock generation resolution	1.0 to 1.5 GHz (in steps of 100 kHz) 1–32 dividers (in steps of 1)
<b>Input/Output reference clock</b>	Input reference clock options	<ul style="list-style-type: none"> <li>Onboard VCxO</li> <li>Onboard VCxO continuously matched with GPS</li> <li>External</li> </ul>
	Onboard VCxO frequency	10 MHz
	Onboard VCxO precision	<ul style="list-style-type: none"> <li>Matched to GPS reference: &lt; 0.1 ppm</li> <li>Free running: 2.5 ppm</li> </ul>
	Onboard VCxO phase noise	<ul style="list-style-type: none"> <li>10 Hz: –83 dBc/Hz</li> <li>100 Hz: –115 dBc/Hz</li> <li>1 kHz: –135 dBc/Hz</li> <li>10 kHz: –140 dBc/Hz</li> </ul>
	Output reference clock	Same as selected reference clock
	Input/Output reference clock impedance	50 $\Omega$
	Input/Output reference clock type	Single-ended LVCMOS (10 dBm)
	Input/Output reference clock connectors	MMCX
<b>Input external clocks</b>	Input external clock type	Single-ended LVCMOS (10 dBm)
	Input external clock impedance	50 $\Omega$
	Input/output external clock connectors	MMCX
	Input external clock range	From 1 MHz to 1 GHz
<b>GPS</b>	Antenna localization	<ul style="list-style-type: none"> <li>Near a window (installation dependant)</li> <li>Outdoors</li> </ul>
	Required antenna specifications	3.3 V active antenna
	Antenna input connector	SMA
	Antenna input impedance	50 $\Omega$
	PPS output connector	MMCX
	PPS output impedance	50 $\Omega$
<b>Host programming interface</b>	cPCI (PXI compatible)	<ul style="list-style-type: none"> <li>33 MHz/66 MHz</li> <li>16 bits/32 bits</li> </ul>
	<b>Front panel GPIO-32 interface</b>	<ul style="list-style-type: none"> <li>3.3 V</li> <li>LVCMOS</li> </ul>
<b>Front panel GPIO-32 interface</b>	Interface	<ul style="list-style-type: none"> <li>3.3 V</li> <li>LVCMOS</li> </ul>
	Connector	<ul style="list-style-type: none"> <li>2 <math>\times</math> 17 header</li> <li>Pitch 0.05 in.</li> </ul>

# Block diagrams



# Typical Lyrtech system configuration example

## Synchronous, multichannel acquisition system



### FOR MORE INFORMATION

#### Lyrtech Inc.

2800 Louis-Lumière Street, Suite 100  
 Quebec City, Quebec  
 G1P 0A4 CANADA

**Phone:** (1) 418-877-4644 (international)  
 1-888-922-4644 (toll free USA and Canada)

**Fax:** (1) 418-877-7710

[www.lyrtech.com](http://www.lyrtech.com)

[info@lyrtech.com](mailto:info@lyrtech.com)

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2009-06

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