

## 4×SFP/SFP+ Quad-port, straight SFP/SFP+ FMC module

- ❖ Versatile and industry-standard VITA 57.1 FMC module
- ❖ Four, front panel SFP/SFP+ ports
- ❖ Supports multiple clock options
- ❖ Up to four OBSAI/CPRI interfaces
- ❖ Perfect for Lyrtech's  $\mu$ TCA Perseus AMCs



PICTURE TO COME

The 4×SFP/SFP+ FPGA mezzanine card (FMC) directly interfaces four multigigabit transceivers of the FPGA to SFP/SFP+ transceiver modules. Each SFP/SFP+ transceiver supports fiber optic or copper interfaces for high-speed protocols such as OBSAI/CPRI and others.

The 4×SFP/SFP+ FMC is also compatible with the Virtex-6's signaling scheme through its use of voltage translators on the control signals.

The 4×SFP/SFP+ complies to the VITA 57.1 standard, widely used by the digital signal processing industry, making it easier for developers to integrate FPGAs to their embedded system designs. The 4×SFP/SFP+ is ready for use with Lyrtech's  $\mu$ TCA Perseus AMCs, but it can as easily be used on other AMCs.

The four front panel SFP/SFP+ ports extend slightly outward from the front panel to comply with the mechanical specifications for FMCs.

### Hardware architecture

The VITA 57.1 (FMC) standard comes to the rescue of complex designs with its unprecedented mechanical and electrical flexibility — VITA 57.1 provides a standard specification for small mezzanine modules designed to adapt an FPGA-based carrier card to different I/O requirements.

### Features

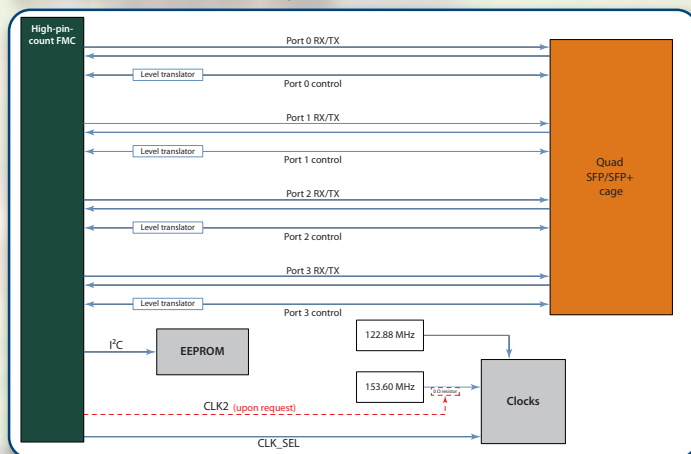
- Quad SFP/SFP+ front panel cage
- Direct interface to the FPGA's high-speed transceivers for maximum bandwidth and minimum latency
- Default OBSAI/CPRI clock configuration and software selection
- Other standard protocols can be configured upon request (contact [Lyrtech](http://www.lyrtech.com) for details).

### Clock management

The module is equipped with two onboard, low-jitter, fixed, 122.88 MHz or 153.60 MHz reference clocks. When

**Infinite possibilities...**

4×SFP/SFP+ functional block diagram



it is not installed, 153.60 MHz clock source, can be selected from the FMC. The clock is buffered and distributed to both M2C clock outputs and to GBTCLK0 and GBTCLK1. To synchronize several modules, select a user clock with the clock buffer originating from the FMC's CLK2 (requires a special configuration where the 153.60 MHz oscillator must be removed. Discuss it with [us](mailto:us)).

4× SFP/SFP+ clock modes block diagram

